REMARKS

The application has been reviewed in light of the final Office Action dated April 11, 2005. Claims 1, 2 and 10-15 are pending, with claims 1 and 10 being in independent form. Claims 3-9 were previously canceled, without prejudice or disclaimer.

Claims 1, 2 and 10-15 were rejected under 35 U.S.C. §102(e) as purportedly anticipated by U.S. Patent No. 6,853,063 to Akiyama et al. Claims 1, 2 and 10-15 were rejected under 35 U.S.C. §103(a) as allegedly unpatentable over U.S. Patent No. 5,245,215 to Sawaya in view of U.S. Patent Application Publication No. 2003/0001808 A1 (Sakuma et al.).

Applicant has carefully considered the Examiner's comments and the cited art, and respectfully submits that independent claims 1 and 10 are patentable over the cited art, for at least the following reasons.

This application relates to a semiconductor device integrating a plurality of semiconductor chips into a single package which is responsive to different signal levels (for example, 5 volt high level signals and 3.3 volt high level signals). Such a semiconductor device may include, for example, a primary side chip responsive to one signal level and a secondary side chip responsive primarily to another signal level.

Applicant devised a semiconductor device which integrates a plurality of semiconductor chips into a single package. A first (for example, primary side) semiconductor chip in the semiconductor device outputs one or more first signals having a first level. A second (for example, secondary side) semiconductor chip in the semiconductor device includes a signal level conversion circuit which converts the first signals from the first

semiconductor chip into second signals having a second level different from (for example, higher than) the first level. Thus, the first semiconductor chip can operate at a lower voltage level, and the second semiconductor chip is nevertheless able to output signals at the second (higher) level which are acceptable to a device which operates at the second level. Each of independent claims 1 and 10 includes these features.

Akiyama, as understood by Applicant, is directed to a multi-chip type semiconductor device for a communication terminal. The semiconductor device of Akiyama is fabricated by standard manufacturing technologies and LSI assembly processes, and each LSI in the package needs to be insulated. Thus, high capacitive insulation is provided to each of the last stage of two adjacent LSIs (for example, primary side circuitry and secondary side circuitry) in need of electrical separation and isolation.

A graphical comparison of the semiconductor device of Akiyama and a semiconductor device according to one exemplary embodiment of this application is attached hereto as Exhibit A.

Both of the primary side circuitry and the secondary side circuitry operate at 3.3V (see Akiyama, column 5, lines 47-51).

Applicant does not find disclosure or suggestion in Akiyama, however, of a semiconductor device which integrates a plurality of semiconductor chips into a single package comprising a first semiconductor chip which outputs one or more first signals having a first level, and a second semiconductor chip which includes a signal level conversion circuit, wherein the signal level conversion circuit converts the first signals from

the first semiconductor chip into second signals having a second level different from the first level of the first signals, as provided by the claimed invention of independent claims 1 and 10.

Should the Examiner disagree therewith, Applicant requests that the Examiner cite to the specific column and line numbers in the cited reference where basis for the disagreement can be found.

Sawaya, as understood by Applicant, is directed to a method of manufacturing a multi-chip packaged semiconductor device. A plurality of LSIs are installed by being flipped on a simple frame such that each of the LSIs is provided with a bump at its pad portion. A flexible substance such as a FPC (flexible printed circuit) is installed on the LSIs to make contact with the bumps and external lead frames from the LSIs, so that connections of the LSIs of the multi-chip package are made without conducting bonding works.

However, Sawaya is not directed at the problem that some chips operate at one level while other chips operate at a second level which is different from the first level. The Office Action acknowledges that Sawaya does not teach or suggest a signal level conversion circuit, wherein the signal level conversion circuit converts first signals having a first level into second signals having a second level different from the first level, as provided by the claimed invention of the present application.

Sawaya is clearly very different in purpose and structure from the claimed invention of this application.

Sakuma, as understood by Applicant, is directed to a method of manufacturing a LCD

(liquid crystal display) panel. When a plurality of drivers are energized at the same time to drive a LCD, generally, an overcurrent flows through a power supply circuit and therefore a protection circuit is activated to shut down the power supply circuit. The method of Sakuma avoids the occurrence of the overcurrent, and more specifically, the powers for the plurality of drivers are energized with a slight delay from each other. An amount of a current flow at a time is thereby limited to one of the plurality of drivers.

Accordingly, Sakuma is concerned with control of current flow and not with signal level conversion.

Moreover, Sakuma does not disclose or suggest a signal level conversion circuit which converts first signals from a first semiconductor chip into second signals having a second level different from the first level of the first signals, as provided by the claimed invention of independent claims 1 and 10.

Applicant submits that since the purposes of Sawaya and Sakuma are very different from that of the claimed invention of this application, the claims simply would not have been obvious from the Sawaya and Sakuma references.

Applicant does not find disclosure or suggestion in the cited art of a semiconductor device which integrates a plurality of semiconductor chips into a single package, comprising a first semiconductor chip which outputs one or more first signals having a first level, and a second semiconductor chip which includes a signal level conversion circuit, wherein the signal level conversion circuit converts the first signals from the first semiconductor chip into second signals having a second level different from the first level of the first signals, as

provided by the claimed invention of independent claims 1 and 10.

In view of the remarks hereinabove, Applicant submits that the application is now in condition for allowance. Accordingly, Applicant earnestly solicits the allowance of the application.

If a petition for an extension of time is required to make this response timely, this paper should be considered to be such a petition. The Office is hereby authorized to charge any fees that may be required in connection with this response and to credit any overpayment to our Deposit Account No. 03-3125.

If a telephone interview could advance the prosecution of this application, the Examiner is respectfully requested to call the undersigned attorney.

Respectfully submitted,

Paul Teng, Reg. No. 40,837
Attorney for Applicant
Cooper & Dunham LLP
Tel.: (212) 278-0400